EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Andrew Wright on 3/23/2010.

The application has been amended as follows (next page):

1. A method of semiconductor fabrication, comprising the steps of:

forming a sidewall image transfer (SIT) loop on a substrate such that the SIT loop forms a hard mask having a width substantially equal to a critical width of a narrow section of a target shape, wherein the narrow section of the target shape corresponds to a pair of critical edges of the hard mask formed by the SIT loop;

protecting a the pair of critical edges of the hard mask on the substrate with a first portion of a follow-on mask, wherein a width of the first portion of the follow-on mask exceeds the critical width by an amount of overlap, and a width of a wide section of the follow-on mask exceeds a width of a wide section of the target shape;

removing an exposed portion of the hard mask that is not covered by the follow-on mask; and

exposing the pair of critical edges of the hard mask by etching the follow-on mask to reduce the width of the first portion of the follow-on mask to less than the critical width.

8. A method of semiconductor fabrication, comprising the steps of:

forming a sidewall image transfer (SIT) loop on a substrate such that the SIT loop forms a hard mask, wherein a width of the hard mask substantially equals a width of a narrow section of a target shape, and wherein the narrow section of the target shape corresponds to a pair of critical edges of the hard mask formed by the SIT loop;

forming a follow-on mask in a loop-cutter pattern on a portion of the hard mask, wherein the follow-on mask comprises a wide-image section having a width that exceeds a width of a

wide section of the target shape and a narrow-image section having a width that exceeds the width of the hard mask;

removing a portion of the hard mask left exposed by the follow-on mask; and

removing at least a portion of the narrow-image section of the follow-on mask.

21. (Currently Amended) A method of combining a wide-image mask and loop-cutter mask, comprising the steps of:

forming a sidewall image transfer (SIT) hard mask loop on a substrate, wherein a width of a narrow section of a target shape substantially equals a width of the hard mask loop, the narrow section of the target shape corresponds to a pair of critical edges of the SIT hard mask loop, and a width of a wide section of the target shape exceeds the width of the hard mask loop;

forming a follow-on mask over a portion of the hard mask loop, wherein the follow-on mask includes a first section corresponding to the wide section of the target shape and a second section overlapping the narrow section of the target shape, and a width of the second section of the follow-on mask exceeds the width of the narrow section of the target shape;

removing regions of the hard mask loop uncovered by the follow on mask;

etching the second section of the follow-on mask to expose underlying edges of the hard mask loop;

etching the first section of the follow-on mask to reduce its length and width to produce an image pad that substantially conforms to the wide section of the target shape; and

etching the substrate uncovered by the remaining hard mask loop and image pad.

Allowable Subject Matter

2. Claims 1, 4-10, 12-14, 21-28 are allowed.

3. The following is an examiner's statement of reasons for allowance:

4. Regarding claim 1, the cited prior art of record fails to disclose or render obvious a method of semiconductor fabrication comprising the steps of "forming a sidewall image transfer (SIT) loop on a substrate such that the SIT loop forms a hard mask having a width substantially equal to a critical width of a narrow section of a target shape, wherein the narrow section of the target shape corresponds to a pair of critical edges of the hard mask formed by the SIT loop" and "and exposing the pair of critical edges of the hard mask by etching the follow-on mask to reduce the width of the first portion of the follow-on mask to less than the critical width.", in combination with the rest of the steps/limitations of claim 1.

5. Regarding claim 8, the cited prior art of record fails to disclose or render obvious a method of semiconductor fabrication comprising the steps of "forming a sidewall image transfer (SIT) loop on a substrate such that the SIT loop forms a hard mask, wherein a width of the hard mask substantially equals a width of a narrow section of a target shape, and wherein the narrow section of the target shape corresponds to a pair of critical edges of the hard mask formed by the SIT loop" and "removing a portion of the hard mask left exposed by the follow-on mask; and removing at least a portion of the narrow-image section of the follow-on mask.", in combination with the rest of the steps/limitations of claim 8.

6. Regarding claim 21, the cited prior art of record fails to disclose or render obvious a method of semiconductor fabrication comprising the steps of "forming a sidewall image transfer (SIT) hard mask loop on a substrate, wherein a width of a narrow section of a target shape substantially equals a width of the hard mask loop, the narrow section of the target shape corresponds to a pair of critical edges of the SIT hard mask loop. and a width of a wide section of the target shape exceeds the width of the hard mask loop" and "etching the second section of the follow-on mask to expose underlying edges of the hard mask loop; etching the first section of the follow-on mask to reduce its length and width to produce an image pad that substantially conforms to the wide section of the target shape; etching the substrate uncovered by the remaining hard mask loop and image pad", in combination with the rest of the steps/limitations of claim 21.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MAHMOUD DAHIMENE whose telephone number is (571)272-2410. The examiner can normally be reached on week days from 8:00 AM. to 5:00 PM..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. D./

Examiner, Art Unit 1792

/Parviz Hassanzadeh/

Supervisory Patent Examiner, Art Unit 1792